## REMARKS

Claims 10 and 21-40 are pending in the Application.

Claims 10 and 21-40 stand rejected.

## I. OBJECTION TO THE SPECIFICATION

The Examiner has objected to the Specification because the Amendment submitted on August 28, 2002 introduced a reference number (401) not appearing in the drawings. The Applicant has hereinabove amended the Specification to correct the inadvertent change to the correct reference number and correct the typographical error in the Application as originally filed with respect to reference numeral 401. As amended above, the Specification comports with FIGURE 4 in which reference numeral 402 is associated with GHV0.

## II. REJECTION UNDER 35 U.S.C. § 103

Claims 10 and 21-41 have been rejected under 35 U.S.C. § 103 as being unpatentable over *Patt, et al.*, "Alternative Implementations of Hybrid Branch Predictors," Proceedings of the 28th Annual Symposium on Microarchitecture, 1995, pp. 252-257 ("*Patt*") in view of *Giacalone et al.*, U.S. Patent No. 6,272,624 (*Giacalone*). The Applicants respectfully traverse the rejection of claims 10 and 19-41 under 35 U.S.C. § 103.

As an initial matter, *Giacalone* is not prior art. As evidenced by the Declaration Under 37 C.F.R. § 1.131, the claimed inventions existed and worked for their intended purpose prior to April 1, 1999. For at least the reason that *Patt* does not teach a fetch-based history table, nor a fetch-based history table with each entry containing bits representing a prediction value for a plurality of branches in a fetch group, *Patt* does not teach or suggest all of the limitations of claim 10, and claims 21-40 (*See* Paper No. 8, page 3; page 6; page 10.)

Additionally, with respect to claims 10 and 30, it is admitted that *Patt* does not teach 1-bit counters. (Paper No. 8, page 4; page 11.)

The Examiner asserts that *Patt* teaches, *inter alia*, a sets of branch prediction bits stored in said first and second branch history tables, wherein said each said entry in said tables comprises a 1-bit counter . (Paper No. 8, page 2) (citing *Patt* page 252, section 2; page 255, section 4, 4.1 and Figure 2.) Plainly, *Patt* discloses two-bit counters, not one-bit counters. Each of the citations to *Patt* expressly refers to two-bit counters. The Examiner asserts that a two-bit counter "naturally comprises" a one-bit counter. (Paper No. 8. page 2.) The Applicant respectfully disagrees.1 A two-bit counter does not comprise a one-bit counter.2 A two-bit counter has two output bits that are correlated. A one-bit counter has a single output bit, and two one-bit counters have two single output bits, that is the output bits are uncorrelated. The Examiner's assertion is tantamount to stating that the value "10" comprises the value "1" or, equivalently, the value "0," which is contrary to common knowledge.

Moreover, as the Appellant has previously shown, *Patt* cannot be modified to make the invention of claim 10. *Patt* teaches, in particular, a Branch Predictor Selection Table (BPST) having two-bit counters. (Applicant's Reply, page 11) (citing *Patt*, Section 2, page 252.) The teaching in *Patt* with respect to such a BPST discloses hybrid branch prediction schemes in which the counters in the BPST keep track of the currently more accurate predictor for a branch. (*Id.*) The two-level prediction scheme disclosed in *Patt* is a combination of the hybrid scheme with a first level history based on branch history registers (BHRs). (Applicant's Reply, page 11) (citing *Patt*, Section 4.1, page 255.) *Patt* explicitly teaches that the BPST used in the two-level prediction scheme is a table of two-bit counters. just as disclosed in conjunction with the hybrid prediction scheme (*Patt*, Section 4.2, pages 255-56.) As discussed in conjunction therewith, as noted hereinabove, the two-bit counters of the BPST keep track of the predictor which is currently more accurate for a particular

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1 This statement is similar to asserting that a bicycle "comprises" a unicycle. A bicycle is not a unicycle nor does a bicycle "teach" a unicycle because it has two wheels and a unicycle has one.

2 Neither does a two-bit counter disclose a one-bit counter. A two-bit counter is not a one-bit counter, nor is a two-bit counter two one-bit counters.

branch. This is an essential element of the two-level prediction scheme of *Patt*; it provides the second level of history. (*See Patt*, Section 4.1, page 255.)

The Examiner also states that *Giacalone* demonstrates that it was known at the time of the invention to implement counters in any number of bits, and that it would have been obvious to implement the counters in *Patt* as one-bit counters. (Paper No. 8, page 11) (citing *Giacalone,* column 1, lines 41-43.) The teaching referred to simply states that predictions are stored in n-bit saturating counters, and *n* is typically two, and an array of such counters is indexed by the ghist shift register. (*Giacalone*, column 1, lines 41-43.) The Applicant respectfully submits that this teaching is not a suggestion to use one-bit counters in *Patt*.

A *prima facie* showing of obviousness requires, *inter alia*, that there must be a reasonable expectation of success in modifying or combining the references to make the claimed invention. MPEP § 2143. Furthermore, the reasonable expectation of success must be found in the references themselves. *Id.* The Examiner has provided no evidence whatsoever of a reasonable expectation of success. There is nothing in either *Patt* or *Giacalone* that indicates a reasonable expectation of success in combining the references. *Giacalone* makes no reference to combining branch predictors, and consequently, there is no concept of branch prediction selection or a branch predictor selector table. With respect to *Patt*, *Patt* is directed to an empirical study of a hybrid branch selection scheme, and a two-level prediction scheme. (*Patt*, page 252, Section 1.)

Neither is it sufficient to assert that a person of ordinary skill in the art would have been motivated to modify *Patt* to incorporate one-bit counters because it would have been less hardware space and thus money, or a simple design structure. (Paper No. 8, page 11.) Even if, for the sake of argument, it is assumed that this modification leads to less cost or a simpler design structure, this ignores the fact that there may be considerations that outweigh any such advantage. For example, persons of ordinary skill in the art would appreciate that two-bit counters would be more tolerant of a branch going in an unusual direction. The consideration of such tradeoffs are why asserted motivations or suggestions to combine or modify references mist be supported by objective evidence and broad conclusory statements are not evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d

1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1616-17 (Fed. Cir. 1999). Note too, that this is also inconsistent with the motivation to combine or modify the reference asserted in conjunction with claim 27 in which the Examiner asserts that it would be obvious to more gradually adjust the predictor to the more likely future choice, and plainly two-bit predictors are more gradual than one-bit predictors. (*See* Paper No. 8. page 9.)

Considering claim 25, claim 25 depends from claim 21 and recites the branch prediction circuitry thereof in which the plurality of selection bits [as recited in claim 21] are operable for selecting a first subset of prediction values from the bimodal branch history table and a second subset of prediction values from the fetch-based branch history table. *Patt* allegedly teaches the limitation of claim 25 however, *Patt* only discloses a selector table that selects a single predictor per index. (*Patt*, Section 4.2, page 256.) In other words, *Patt* does not teach predicting more than a one branch per table access, and therefore does not, and cannot teach selecting a first subset of prediction values from the bimodal branch history table and a second subset of prediction values from the fetch-based branch history table. Likewise, *Giacalone*, which does not teach combined predictors cannot teach the limitation of claim 25 either. Thus, the Applicant respectfully disagrees that the references, alone or in combination teach or suggest the limitations of claim 25.

With respect to claim 31 directed to the processing system of Claim 28 in which the first and second branch history tables and said selector table form a portion of a branch execution unit. The Applicant respectfully traverses the taking of Official Notice that "it was known at the time of the invention to implement unit circuitry of elements with related functionality." (Paper No. 8, page 12.) The noticed facts do not address the limitation of claim 31. Furthermore, it is so broad as to be incapable of immediate and unquestionable demonstration. MPEP § 2144.03 The Applicant respectfully requests that such taking of Official Notice be supported by evidence.

In view of the foregoing, the Applicant respectfully requests that the rejection of claims 10 and 21-40 under 35 U.S.C. § 103 be withdrawn.

III. CONCLUSION

As a result of the foregoing, it is asserted by the Applicants that the remaining claims in the Application are in condition for allowance, and respectfully request an early allowance of such claims.

Applicant respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

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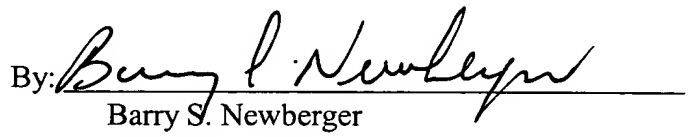
By: 
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